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A Simple Algorithm for SRF Theory with Three Phase Shunt Active Power Filter

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Abstract. Shunt Active Power Filters (APFs) are the up-to-date solution to power quality problems. Harmonic reference detection is the key word for the proper operation of shunt APF. One of the most famous detection control schemes for shunt APFs is the Synchronous Reference Frame (SRF). In this paper, two new modifications of (SRF) detection control scheme are presented. The first modification is done by introducing a new scheme for the dc bus control loop. The second modification is accomplished by implementing the SRF without load current sensors and using only the supply current sensors. These improvements, compared to the conventional (SRF), simplify the control system, minimize the system delay time, improve the APF performance, and reduce the cost of the system. The simulation results, using MATLAB/SIMULINK, demonstrate the viability and simplicity of the modified control scheme, its success in meeting power quality standards limits, and increasing the accuracy of generated reference signal.

Keywords: Synchronous Reference Frame (SRF), Sampling Time, Active Power Filter (APF).

1. Introduction

The performance of APF is very much dependent on how the reference compensating signals are estimated. Instantaneous reactive power theory [1,2], modified p-q theory [2,3,4], synchronous reference frame(SRF) theory [2,5,6], instantaneous i_d-i_q theory [2,7], and method for estimation of current reference by maintaining the voltage of dc link [8] were generally reported in literature for estimation of harmonic current references for APF through subtraction of positive sequence fundamental current component from the load current. These control schemes look very attractive for their simplicity and ease of implementation, but the drawback of any control algorithm is the non negligible time it takes to obtain the system waveforms via transducers for voltage and current, to sample the currents and voltages of a system, to do calculations on the digitized signals, to derive reference quantities according to some non sinusoidal power theory, and to convert the digitized reference signals back to analog signals (if necessary). In addition to this, the sampling rate forces a stepwise output which further delays the output signal. Increasing the sampling rate may again lower the processing speed. Fundamentally, there will always be a delay of the reference with sampling and digital signal processing, due to the abovementioned reasons.

This may affect the system performance in two aspects [9]: 1) the delay will cause non-ideal compensation (will not compensate all non-active power or 2) the system will lose the ability to compensate for dynamic changes (when the reference is deliberately delayed with one sampling period to output the reference precisely in phase with the next period). This section indicates how these issues have to be evaluated to optimize/minimize the delay time. The minimization of control system delay is achieved by reducing the calculation efforts, and so reduces the execution time of the software. Also minimization of the required measurements reduces the A/D software calculation. The reducing of execution time of the software allows the controller to reduce the sampling time. Because the execution time must be lower than the sampling time. The simulation results will show the great effects of minimization sampling time especially in high variation loads.

In this paper, a new simple SRF based scheme is proposed to extract the fundamental active component of the load currents. The proposed method depends on introducing two modifications to the conventional SRF. Compared to the conventional SRF, the proposed system is simple, low cost, fast, and gives high performance (low THD for the source current). The paper starts with introduction (1), then describes the system under study and its parameters in the Matlab, (2). The conventional SRF theory is reviewed in (3). In (4), the simulation results for the conventional SRF are discussed. In (5), a simplification for the DC bus control loop is introduced. In (6) another modification removes the load current sensors. Section (7) is the conclusions. (8) and (9) are the appendix and references paragraphs respectively.

2. Matlab Based Simulation

The power source, rectifier fed resistive load, unbalanced load and active filter is modeled in MATLAB using Power System Block set. Figure (1) depicts the test bench to estimate the performance of the active filter with proposed control scheme. The source block consists of three-phase voltage source with small impedance representing a stiff source to gauge the performance of the active filter with proposed scheme. The set of load consists of diode rectifier and delta connected resistive load with unequal arms. The non linear load has been modeled as diode rectifier feeding resistance, which represents the real power consumed by the load. The unbalance in the load currents has been generated by the three phase delta connected resistive load.

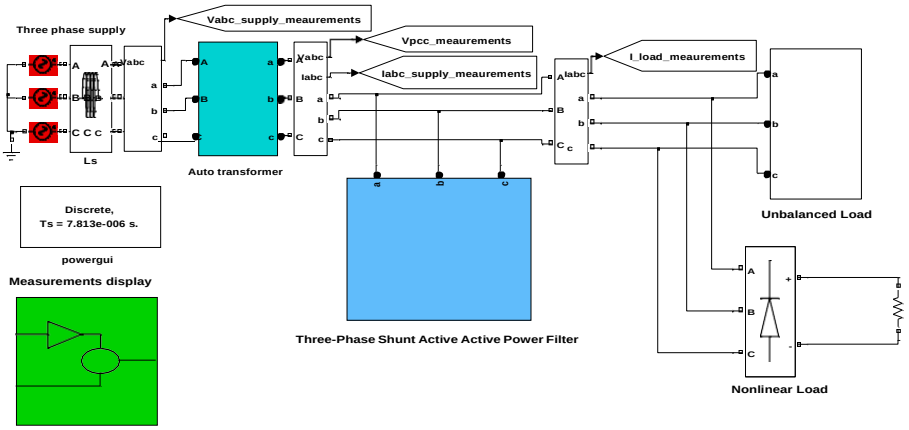


Fig. (1). Main block of proposed control scheme with APF under MATLAB

The Shunt Active Filter consists of two main parts: a) The Inverter, b) The controller. The controller is fed with the measurements from the main system in addition to the inverter currents and the voltage of the DC side of the inverter. The controller function is to produce the switching scheme of the switches (IGBT's) of the inverter. Also, it gives the signal required for the initial charging of the capacitor in the DC side of the inverter.

The inverter consists of three modules; each consists of two IGBT's connected in series with their anti- parallel diodes. The DC side is a capacitor bank (C= 900 μF). The capacitor bank is first charged from the main system supply through the charging resistance (R= 15Ω) with the diodes acting as an uncontrolled rectifier bridge. After some time, this resistance is disconnected from the circuit by a contactor, thus short circuiting the resistance. Also, a line inductor is used at the output of each module in order to smooth the inverter current. Forward voltages of IGBT devices and diodes are 2.8V and 1V respectively. The switching times of

IGBT are 3μs. Table (I) presents the parameters of the simulated system. It must be noted that, the delay time in the feedback signals of the real system must be considered in the simulation system of APF. This time is used by the digital control system to obtain the system voltages and currents via transducers, to sample the currents and voltages, and to convert the signal back to analogue signal (driving signal). This time is set to be 15μsec. in this simulation work as it is -for example- in the DSP kit (TMS320F2812 eZdsp).

3. Basic SRF Theory

It is proposed to use SRF theory [6, 10] to extract instantaneously active components positive sequence of currents at the fundamental frequency. The SRF isolator extracts the fundamental

component of the load current by transformation of load currents: i_{La}, i_{Lb} and i_{Lc} to d-q reference frame. In the synchronously rotating reference frame, the positive sequence components at fundamental frequency (ω_1), are transformed to DC quantities and all harmonic and negative frequency components undergo a frequency shift of ω_1(=50Hz).

$$\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \tag{1}$$

$$\begin{pmatrix} i_{Ld}^{+} \\ i_{Lq}^{+} \end{pmatrix} = \begin{pmatrix} \cos\omega_1 t & \sin\omega_1 t \\ -\sin\omega_1 t & \cos\omega_1 t \end{pmatrix} \begin{pmatrix} i_{L\alpha} \\ i_{L\beta} \end{pmatrix} \tag{2}$$

SRF isolator extracts the DC quantities by low pass filters (LPF) for each i_{Ld} and i_{Lq}. The extracted DC components $i_{LdcD}{}^{+}$ and $i_{LdcQ}{}^{+}$ are transformed back into first α-β frame and then into a-b-c coordinates to obtain net positive sequence fundamental components as shown below:

$$\begin{pmatrix} i_{L1\alpha}^{+} \\ i_{L1\beta}^{+} \end{pmatrix} = \begin{pmatrix} \cos\omega_1 t & -\sin\omega_1 t \\ \sin\omega_1 t & \cos\omega_1 t \end{pmatrix} \begin{pmatrix} i_{LdcD}^{+} \\ i_{LdcQ} \end{pmatrix} \tag{3}$$

Whereas, the real active component of the positive sequence fundamental frequency current at α-β frame ($i_{L1R\alpha}{}^{+}$, $i_{L1R\beta}{}^{+}$) can be easily made from d-q frame, thus the a-b-c coordinates of real active component at fundamental frequency($i_{L1Ra}{}^{+}$, $i_{L1Rb}{}^{+}$, $i_{L1Rc}{}^{+}$) can be evaluated as below:

$$\begin{pmatrix} i^{+}_{L1R\alpha} \\ i^{+}_{L1R\beta} \end{pmatrix} = \begin{pmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \\ 1 & 1 \end{pmatrix} \begin{pmatrix} 0 \\ i^{+}_{LdcQ} \end{pmatrix} \quad (4)$$

$$\begin{pmatrix} i^{+}_{L1Ra} \\ i^{+}_{L1Rb} \\ i^{+}_{L1Rc} \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & 0 \\ -\frac{1}{\sqrt{2}} & \frac{\sqrt{3}}{2} \\ -\frac{1}{\sqrt{2}} & \frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} i^{+}_{L1R\alpha} \\ i^{+}_{L1R\beta} \end{pmatrix} \quad (5)$$

4. Performance of Proposed Control Scheme

The control scheme for the proposed system is based on the SRF based current decomposition, discussed in the previous section. Figure (2) shows the flow of various control signals and control scheme based on the decomposed components. The control scheme depicted in Fig. (2) also incorporates the command for maintaining the constant average DC bus voltage at the VSI.

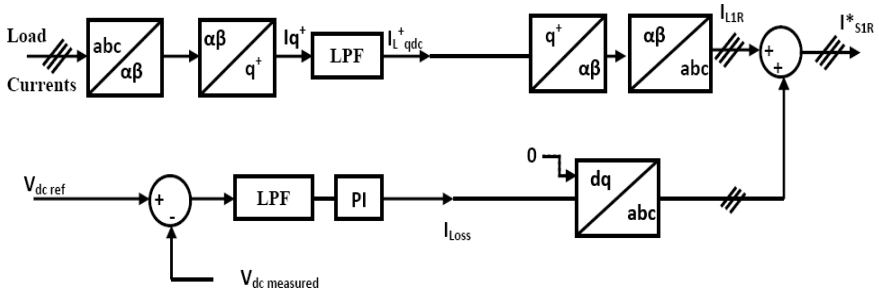


Fig. (2). SRF Control scheme for Active power filter

The command for desired compensation (i_{sa}*, i_{sb}*, i_{sc}*) is derived from taking difference of load current and the other decomposed components need to be compensated. This scheme facilitates the control of APF by indirect current control through hysteresis carrier-less PWM current controller.

A PI controller is used also to regulate the DC bus voltage to its reference value and compensates for the inverter losses. A low pass filter is used to filter the ripples in the feedback path of the DC link voltage. The filtering of DC voltage ensures that power transfer between the DC bus of the inverter and supply takes

place only at fundamental frequency and not as a result of harmonic frequency. To compensate the inverter losses and maintaining the DC bus, the demanded current is added to positive sequence fundamental frequency component of load current, as shown in Fig. (2).

The PWM gating pulses for the IGBTs in VSI are generated by indirect current control using hysteresis current controller over reference supply currents (i_{sa}*, i_{sb}*, i_{sc}*) as in Fig. (3) and sensed supply currents (i_{sa}, i_{sb}, i_{sc}). The controlled compensation current is injected such that the supply current follows the reference current. Hence the source current becomes close to reference currents estimated by SRF decomposer.

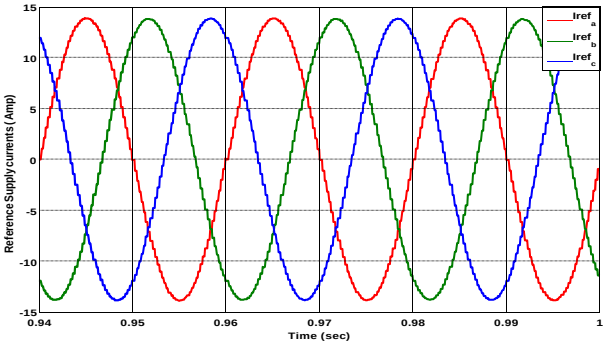


Fig. (3). Reference supply currents

In this section the simulation results will be studied for evaluation of the performance of APF with the proposed control system by analysis through THD of source and load current.

Figure (4) shows the simulation results of the supply current for indirect current control, with the system parameters given in Table (1). Figure (5) shows the harmonics spectrum of load and supply currents.

Table (1). the parameters of the simulated system.

Total Line impedance	L_s=0.733 mH,R_s=0.1Ω
Unbalanced load	R_{ab}=67 Ω, R_{cb}= R_{ca}= 135 Ω
Nonlinear load (rectifier with resistive load R_{dc})	R_{dc}=20Ω
Coupling Impedance	L_f=2mH,R_f=1.0Ω
Dc bus voltage	400 V
Sampling frequency	12.8 kHz
Max switching frequency	12.8 kHz
Hysteresis band(hb)	0.4 A
Dead time between switches	8μs
Line frequency	50 Hz
Mains voltage per phase	100 V

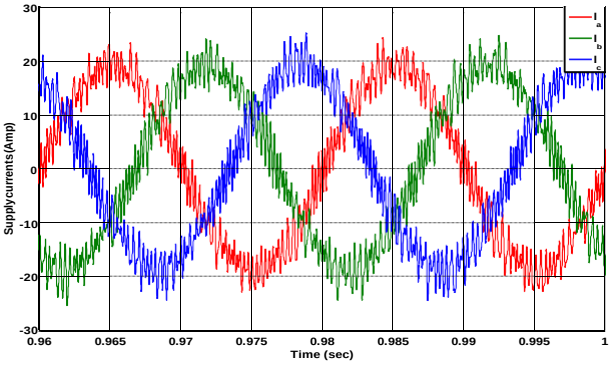
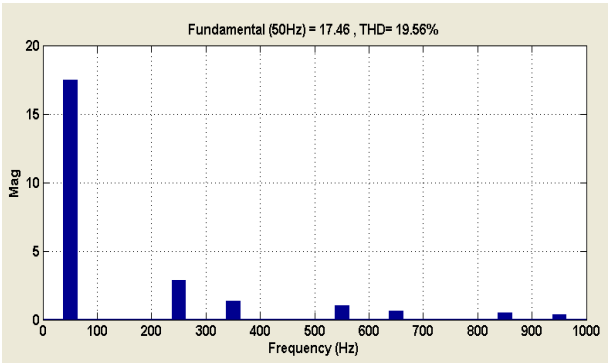
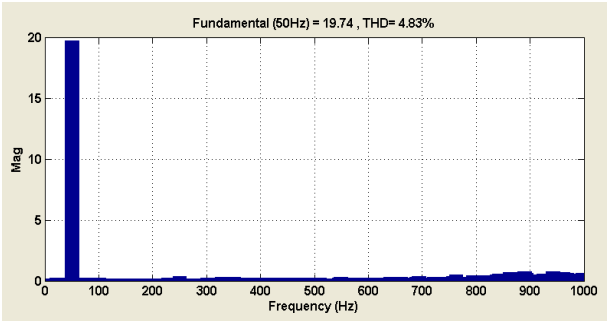


Fig. (4). Three phase supply currents (conventional SRF)



a) Load current harmonic spectrum



a) Supply current harmonic spectrum

Fig. (5). Harmonic spectrum for load and supply currents (peak values)

The bus voltage as shown in Fig. (6) is constant and equals to a preset value, 400 volt. The maximum fluctuation observed is 20 volts, which is good agreement with the design value, where a voltage regulation ratio of ±5% was imposed.

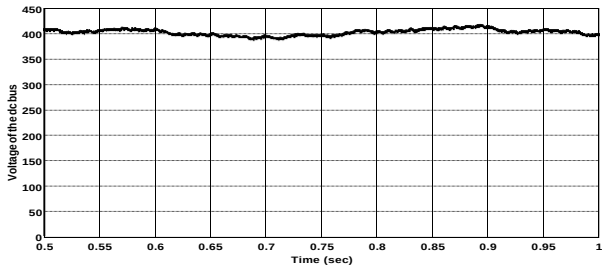


Fig. (6). DC bus voltage

It can be seen that the compensation results respect the IEEE 519 standard for Harmonics [11] (THD ≤5%).

Figure (7) shows the phase shift between supply voltage and current. The supply current is in phase with supply voltage with unity power factor. Figures (8 and 9) show the performance of active power filter with higher sampling frequency. New sampling frequency equals 25.6 kHz (Ts=39.0625μs).

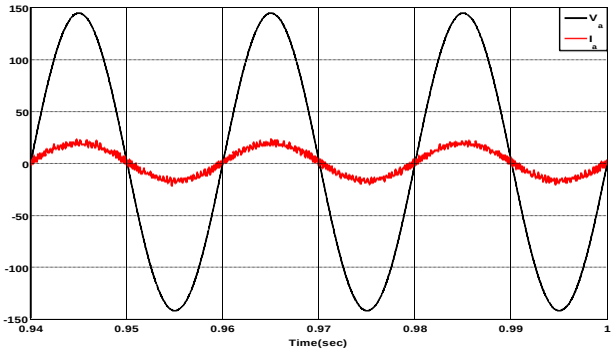


Fig. (7). Voltage and supply current of phase A.

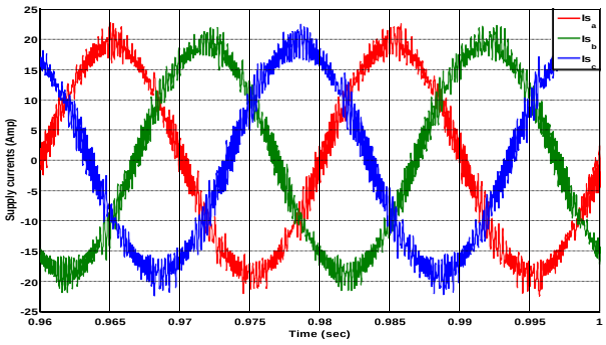


Fig. (8). Three phase supply currents ($f_{sampling}$= 25.6 kHz)

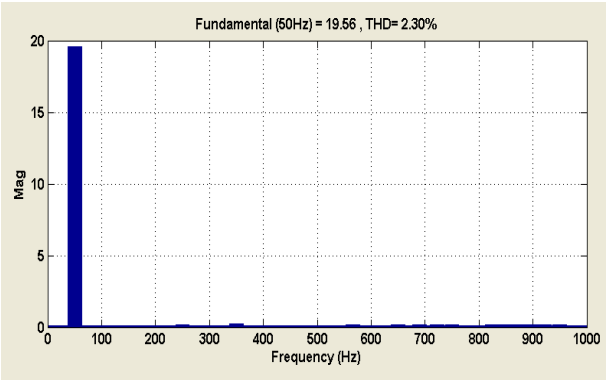


Fig. (9). Harmonic spectrum for supply current ($f_{sampling}$= 25.6 kHz)

Table (3). Compensation results for higher sampling frequency

	THD %			RMS supply currents			Unbalance %	Voltage Regulation %
	Phase "a"	Phase "b"	Phase "c"	Phase "a"	Phase "b"	Phase "c"		
$f_{sampling}$=12.8 kHz	4.83	4.89	3.23	13.7	13.8	13.8	1	4.08
$f_{sampling}$=25.6 kHz	2.3	1.74	2.14	13.5	13.48	13.42	0.59	3.58

According to Table (1). and Fig.(4-9), the performance of the APF is improved with higher sampling frequency. As the sampling time decreases, the switching frequency increase and so the accuracy of calculation increases. Also this will increase the speed response of APF, and the harmonics caused by switching process will be higher than the highest frequency to be eliminated. But in this paper the max switching frequency is limited by 12.8 kHz, as it is depending on the sampling time which is adjusted taking into consideration the required closed loop

computation time of DSP. So, the only method to reduce the sampling time is minimizing the calculations efforts in the reference detection method

To evaluate the modifications of SRF scheme, the control system is simulated. And to show the execution time of the control scheme, the software is compiled to DSP control Board (TMS320F2812 eZdsp). Table (2) shows the delay time (the required execution time) of SRF software.

Table (2). Compensation results

	THD %			RMS supply currents			Unbalance %	Voltage Regulation %
	Phase "a"	Phase "b"	Phase "c"	Phase "a"	Phase "b"	Phase "c"		
Without APF	19.56	19.66	21.63	12.6	12.65	11.4	8	7.2
With APF	4.83	4.89	3.23	13.7	13.8	13.8	1	4.08

Table (4). Execution time of SRF software

Task	Execution time (μ sec)
Measurements and A/D conversion	7
Rescaling calculation*	13
Detection method(SRF)	50
Modulation switching method	15
Total execution method	85

*Rescaling calculations: conversion the measured variables to their actual values.

5. Simplification of DC Bus Control Loop

The first modification in the control scheme is changing the dc bus control Loop. A PI controller is used also to regulate the DC bus voltage to its reference value and compensates for the inverter losses. A low pass filter is used to filter the ripples in the feedback path of the DC link voltage. The filtering of DC voltage ensures that power transfer between the DC bus of the inverter and supply takes place only at fundamental frequency and not as a result of harmonic frequency. To compensate the inverter losses and maintaining the DC bus, the demanded current (I_{Loss}) is added to the extracted dc components I_{LdcQ}^{+}. And so, the calculations can be cancelled to convert the error command signal of the dc bus control loop to three phase currents, pure sinusoidal waveforms and in phase with the three phase supply, and adding them to the positive sequence fundamental components of the load currents to get the reference supply currents. Figure (10) and equations 6 and 7 show the modification of the dc bus control loop.

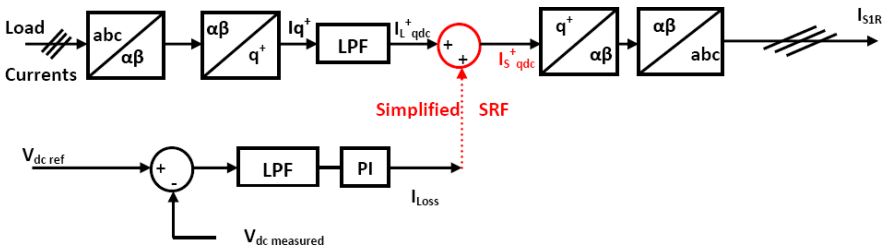


Fig. (10). Block diagram for Simplified SRF method

$$\begin{pmatrix} i_{L\,1R\alpha}^{+} \\ i_{L\,1R\beta}^{+} \end{pmatrix} = \begin{pmatrix} \cos\omega_1 t & -\sin\omega_1 t \\ \sin\omega_1 t & \cos\omega_1 t \end{pmatrix} \begin{pmatrix} 0 \\ i_{LdcQ}^{+} + I_{Loss} \end{pmatrix} \tag{6}$$

$$\begin{pmatrix} i_{L\,1Ra}^{+} \\ i_{L\,1Rb}^{+} \\ i_{L\,1Rc}^{+} \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & 0 \\ -\frac{1}{\sqrt{2}} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{\sqrt{2}} & \frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} i_{L\,1R\alpha}^{+} \\ i_{L\,1R\beta}^{+} \end{pmatrix} \tag{7}$$

Figure (10) shows that the calculation efforts can be cancelled in the block of dq/abc (dashed line) to convert the losses current into three phase sinusoidal currents in phase with the supply voltages. And so, the losses current can be added directly to the q_{dc} components of the load current.

Figures (11 and 12) as well as table (5), show the simulation results of the Simplified SRF method. Table V shows the improvement in compensation results of the simplified control scheme, and this is because that, the reducing of calculations minimizes the percentage error in the generated reference current. As the cancelled block which concerns with the synchronization with supply voltages; doesn't generate three phase signals typically in phase with the generated signals which represent the active components of the load currents. This error in phase-shift will affect the accuracy of reference signal. While, in the simplified SRF the losses current signal which represented by a dc signal added to another dc signal (q_{dc}).And so, the error due to the difference in phase shift in SRF can be cancelled.

Table (5). Compensation results (simplified SRF)

	THD %			RMS supply currents			Unbalance %	Voltage Regulation %
	Phase "a"	Phase "b"	Phase "c"	Phase "a"	Phase "b"	Phase "c"		
Without APF	19.56	19.66	21.63	12.6	12.65	11.4	8	7.2
SRF method	4.83	4.89	3.23	13.7	13.8	13.8	1	4.08
Simplified SRF method	**3.36**	**4.02**	**4.05**	**13.13**	**13.12**	**13.09**	**0.15**	**3.5**

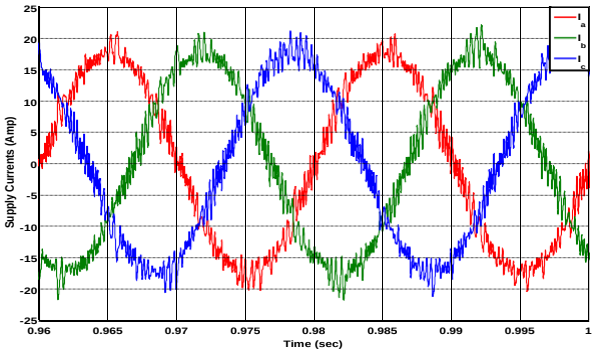


Fig. (11). Three phase supply currents (Simplified SRF)

Figure (12) shows the phase shift between supply voltage and current. The supply current is in phase with supply voltage with unity power factor.

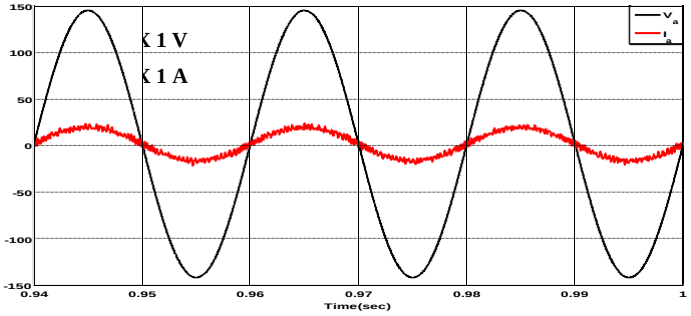


Fig. (12). Voltage and supply current of phase A (Simplified SRF)

The software is tested to show the effect of this modification on the execution time as shown in Table (6).

Table (6). Execution time of simplified SRF software

Task	Execution time (μ sec)
Measurements and A/D conversion	7
Rescaling calculation	13
Detection method(SRF)	30
Modulation switching method	15
Total execution method	65

It can be seen the effect of this modification on reducing the execution time of SRF method, and so the sampling time can be reduced to get more accurate reference signal.

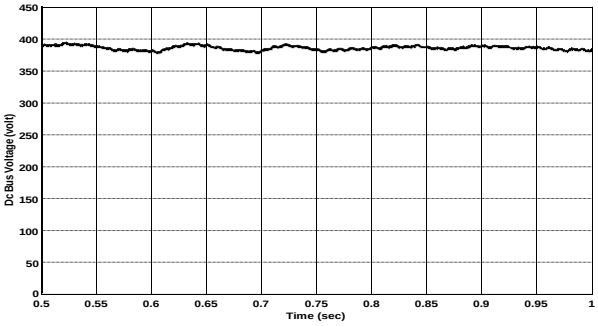


Fig.(13). Dc bus voltage (Simplified SRF – Vdc ref=380)

6. Simplification of SRF Control Scheme without Load Current Sensors

In this section, a new control system is presented based on the theory of SRF detection method. In case of full compensation of all non active components of current, the SRF can be simplified to extract only the positive sequence component of current. Figure (14) shows the basic block diagram of implementation the SRF method in real time systems. The factors K_1 and K_2 represent the gains of the used transducers. To achieve an accurate operation of the hysteresis modulator, it is important to make sure that these gains (K_1 and K_2) are identical. Because the gain K_1 affects the value of reference supply current and the gain K_2 affects the value of actual supply current. But making these gains identical in real time system is very difficult. The proposed modification of the control system is implementing the SRF without load current signals and using only the supply current signals for both extracting the reference current signal and as a feedback of actual supply currents. Figure (15) shows the new control scheme block diagram.

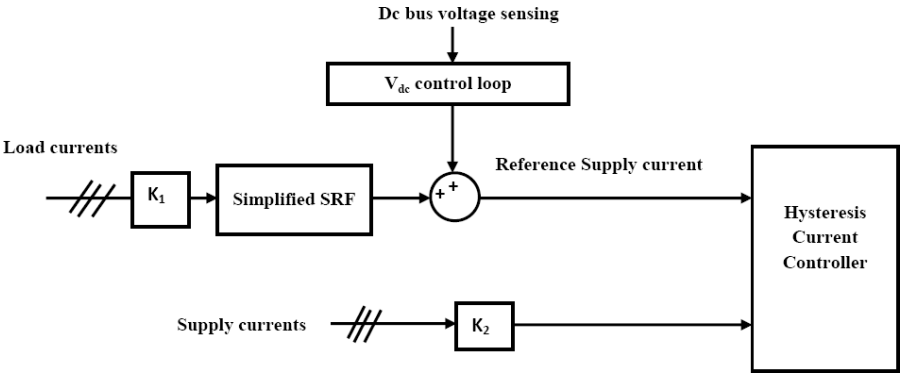


Fig. (14). Block diagram for SRF with load and supply current sensors

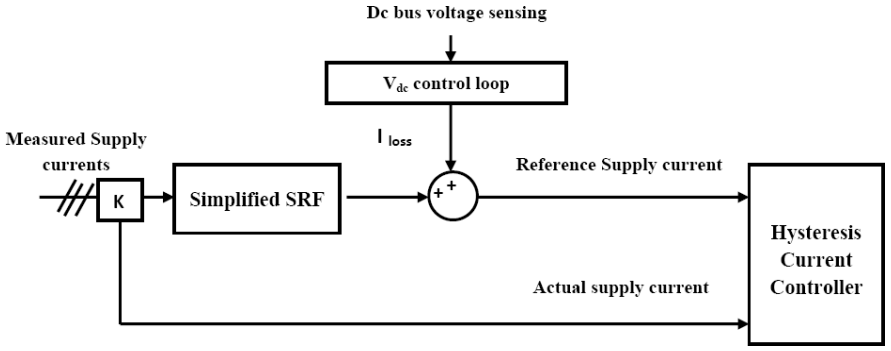


Fig. (15). Block diagram for SRF without Load current sensors

Using of the supply currents sensors, only in the control scheme, overcomes the problem of non identical transducers gains and their effect on the two inputs of the hysteresis modulator. The SRF is used to extract the fundamental active components of the supply current. And the losses of the inverter are presented in terms of the variation of the dc bus voltage .To compensate the losses and maintaining the dc bus voltage constant the demand current (I_{Loss}) is added to the positive sequence fundamental frequency component(q_{dc}^{+}). The optimized new control scheme is simulated under MATLAB/SIMULINK to validate the effectiveness of its theory.

Figure (16) shows the dc bus voltage for the new control system. It is noticed a high fluctuation (70 volts) in dc bus voltage which may lead to unstable operation of APF.

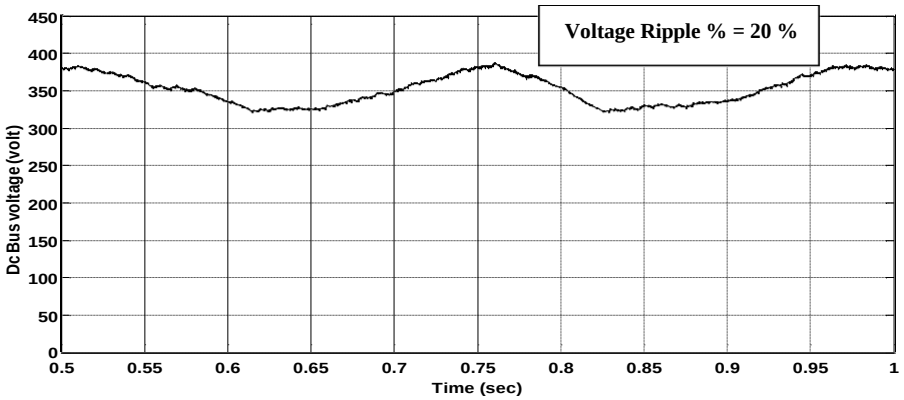


Fig. (16). DC bus voltage (SRF without Load current sensors) – Vdc ref=320

The high fluctuation in the dc bus voltage is occurred as the supply current is used to extract the reference signal, and also as a feedback current for the hysteresis modulator. A sample of supply current is decomposed to detect the load current fundamental active component. The losses of the inverter are drawn from the supply by adding the current I_{Loss} to the fundamental current.

In the next sample, the supply current is decomposed to load active current component and the losses supplied to the inverter, and the dc bus voltage hasn't reached yet to the required reference value and this means the control system will add a new losses current to the reference supply current. After many sample the dc bus will be higher than the reference value, and this means the losses current is to be injected to the supply, by subtracting it from the reference supply current, but the fundamental component of the supply current is containing the fundamental component of the load current and losses that are supplied to the inverter in the previous samples. Subtraction the new losses current will not decrease the reference current to its required value, and this will lead to high reference current and the controller will force the inverter to draw current from the supply .And so, the voltage of dc bus voltage increases again. This accumulation of losses causes a high fluctuation of dc bus voltage and unstable operation of APF.

To overcome this problem, the dc bus voltage control loop is sampled with lower rate than the sampling rate of supply current, i.e. 10 samples of current to one sample of dc bus voltage, and the lowering of sample rate give the system efficient time to supply the losses of the inverter without accumulation the losses in the supply current.

Figure (17) shows the idea of multi-sampling rate system to overcome of the problem of instability of the system due to the accumulation of losses signal. The multi-sampling rates give the dc bus control loop the chance to reset itself.

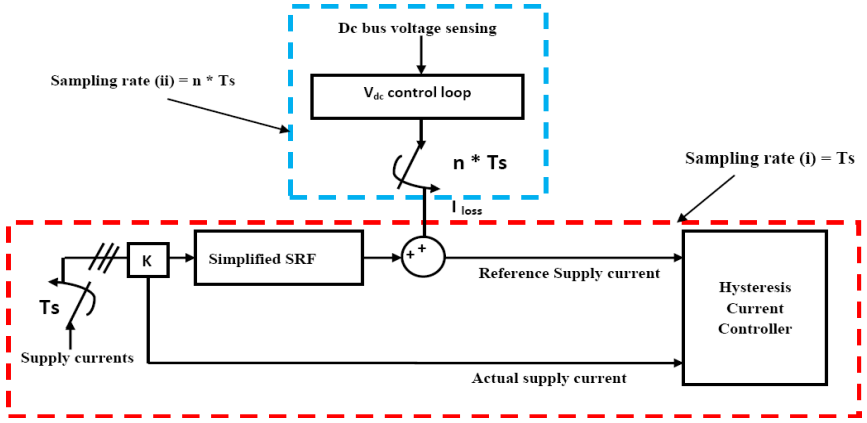


Fig. (17). Block diagram for optimized SRF with multi-sampling rate system.

Figure (18) shows the dc bus voltage with high sampling time (n*Ts), where n =13 with Ts =78.125 µsec. It can be seen that the ripple the dc bus voltage doesn't exceed 10 volt(3%). Sampling rate (i) =78.125 µs and sampling rate (ii) ≈1 ms.

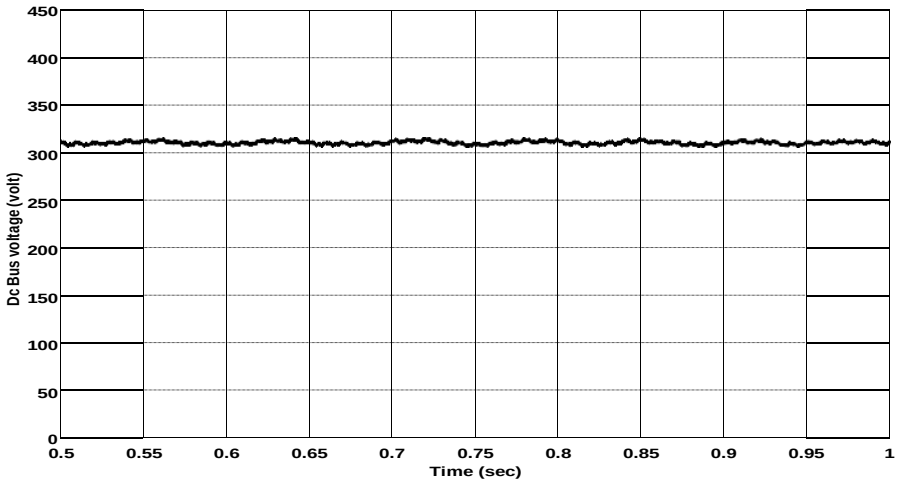


Fig. (18). DC bus voltage (Optimized SRF with multi-sampling rate system)

If the sampling rate (i) = 39.0625 µs, the dc bus is regulated with 10 volts ripple when the sampling rate (ii) = 1msec. It is noticed that the sampling rate (ii) is constant and independent of sampling rate of the current. The highest harmonics order of the load currents to be eliminated is 1050 Hz. The ripple on the dc bus voltage is

mainly occurred by the harmonics components in the inverter current which is injected to the system to compensate the harmonics component in the load current. And so, the variations in the dc bus voltage can be detect with sample for each cycle of the highest frequency component (i.e. sampling time = 1/1000=1 ms). Figures (19 and 20) show the compensation results of optimized SRF with multi-sampling rate system. From the previous figure, it can be seen the effectiveness and stability of the new control scheme. Table (7) shows that the compensation complies with power quality standards for voltage harmonics, regulation and unbalanced currents.

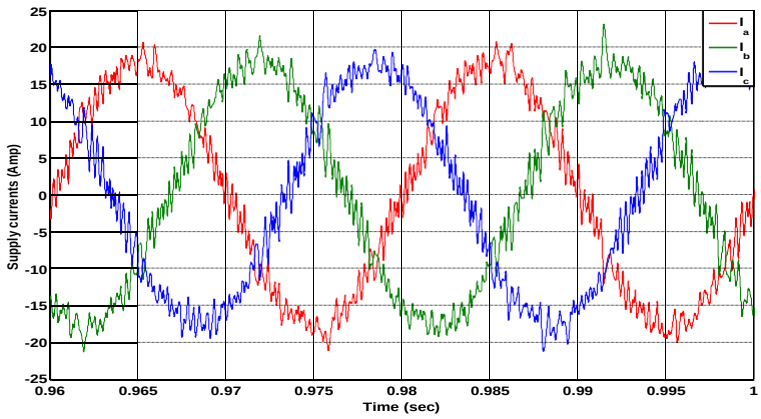


Fig. (19). Three phase supply currents (Optimized SRF with multi-sampling rate system)

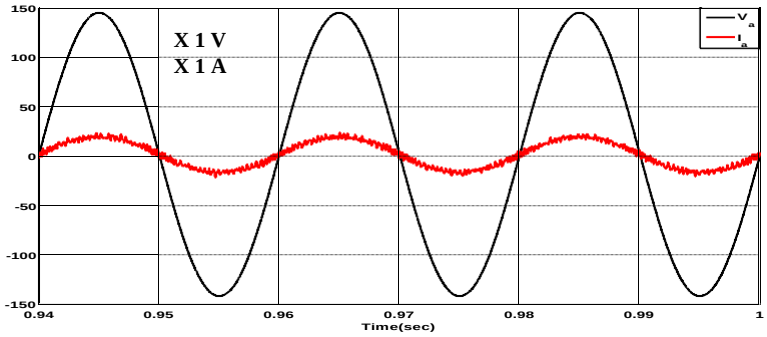


Fig. (20). Voltage and supply current of phase A (Optimized SRF)

Table (7). Compensation results (optimized SRF)

	THD %			RMS supply currents			Unbalance %	Voltage Regulation %
	Phase "a"	Phase "b"	Phase "c"	Phase "a"	Phase "b"	Phase "c"		
Without APF	19.56	19.66	21.63	12.6	12.65	11.4	8	7.2
SRF method	4.83	4.89	3.23	13.7	13.8	13.8	1	4.08
Simplified SRF	3.36	4.02	4.05	13.13	13.12	13.09	0.15	3.5
Optimized SRF	**2.09**	**2.4**	**2.21**	**12.53**	**12.55**	**12.55**	**0.1**	**2.8**

It can be seen that the improving of APF performance with the optimized control scheme compared with both SRF and modified SRF methods especially in reducing THD and rms values of supply currents. Figure (21) shows the reference current for: active fundamental component in the load current "Iref (ILR)", new optimized SRF method "Iref (optimized SRF)", and SRF method. It is noticed that the reference currents for SRF and Optimized SRF are higher than the active fundamental component of the load current as these currents contain the losses current that the mains have to supply it .But it can be noticed that the reference current in case of optimized SRF is lower than the SRF method as the reference signal in optimized SRF is extracted from supply current, while in SRF the reference signal is extracted from load current. And surely, the THD of the measured signal affects on the accuracy of reference signal .And it obviously that the reference signal in optimized SRF (THD of measured signal =2.09 %) is more accurate than the reference signal in SRF (THD of the measured signal 19.56 %).So, the accuracy of the reference supply signal plays a great role in improving the performance of active power filter.

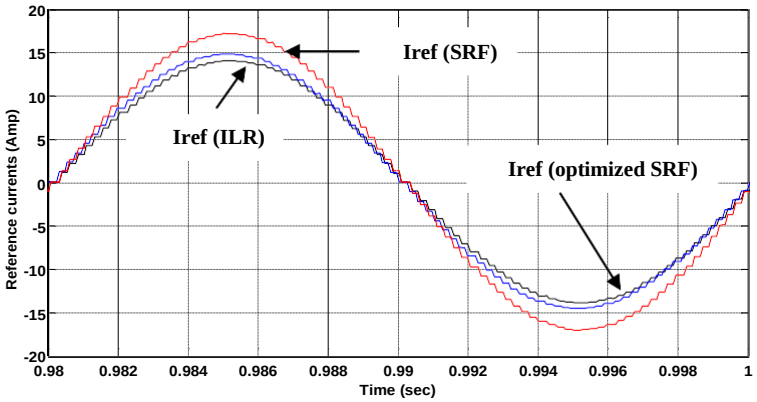


Fig. (21). Reference supply currents (Optimized SRF)

Also the software is tested to show the effect of this modification on the execution time as shown in Table (8).

Table (8). Execution time of optimized SRF software

Task	Execution time (µ sec)
Measurements and A/D conversion	5
Rescaling calculations	8
Detection method(optimized SRF)	22
Modulation switching method	15
Total execution method	50

It can be seen that the effect of this modification on reducing the execution time of SRF method, and so the sampling time can be reduced to get more accurate reference signal. Finally, the advantages of the new optimized SRF method can summarize in some points includes: Fewer required current transducers (only supply current transducers),more accurate reference current signal (less losses and better compensation results),overcome the problem of different transducers gains (K1 and K2), and more simplicity of calculations results in less execution time of software.

7. Conclusion

In this Paper, two modifications of the SRF detection control method of the shunt APF are presented. The system complexity is reduced by introducing a simple DC bus voltage control loop that reduces the program execution time. There is no need to have load current sensors under the same operating conditions to guarantee the same performances. The execution time and THD for the source currents, are compared for each modification alone, together (optimized scheme), with the conventional SRF scheme. The simulation results demonstrate that the optimized

scheme gives the lowest execution time (50 µsec). This means the fastest response, compared to (85 µsec) for the conventional SRF scheme. This gives, also, the most better THD (2.09 %), compared to THD (19.56 %) of the conventional SRF scheme.

The main observation of simulation results is that; the most acting factor which affects the performance of APF, is the reference current detection method and its flexibility for different load conditions. As well as, the number of filters and calculations in detection method and its accuracy in generating the reference currents with lower sampling frequency.

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APPENDIX A:

The unbalance is only in magnitude, which can be measured for the 3- φ systems as follows:-

$$\% \text{ Unbalance} = \frac{\sqrt{(R_m - R_a)^2 + (R_m - R_b)^2 + (R_m - R_c)^2}}{R_m} * 100\%$$

Where R_m is the mean resistance.

خوارزمية بسيطة مع نظرية SRF لمرشح القدرة الفعال ثلاثي الأطوار

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(قدم للنشر في 2018/6/28م؛ وقبل للنشر في 2018/8/0م)

ملخص البحث. تعتبر مرشحات القدرة الفعالة الهتوازية(APFs) هي الحل الحالي لهشاكل جودة القدرة الكهربية. كشف التوافقيات المرجعية هي الكلمة المفتاح للتشغيل السليم لل-APF. واحدة من خطط السيطرة الكشف ألكثر شهرة لـ APFs هو الإطار المرجعي الهتزامن (SRF). في هذه الورقة، يتم عرض تعديلين جديدين في نظرية الـ (SRF)، التعديل ألول يتم عن طريق إدخال خطط سيطرة جديد حلقة التحكم في جهد الـ-DC. ويتم إنجاز التعديل الثاني بتنفيذ SRF دون استشعار الحمل الحالي واستخدام أجهزة الستشعار التيار المصدر فقط. هذه التحسينات، بالمقارنة مع النظرية التقليدية (SRF)، تعمل على تبسيط نظام الرقابة، وتقليل وقت التأخير للنظام، وتحسين أداء APF، والحد من تكلفة النظام. وجاءت نتائج المحاكاة، وذلك باستخدام MATLAB / SIMULINK، بإثبات جدوى و بساطة تعديل خطط السيطرة المقترح، و جناحها في تلبية معايير الجودة العالمية ، وزيادة دقة إشارة مرجعية المولدة.