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Developing a Design Tool for Cooling Microprocessor Hotspots Using Thermoelectric Modules

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Abstract. Keeping a microprocessor surface temperature evenly distributed and below a threshold value is difficult to achieve using conventional electronic cooling approaches. Hotspots on the microprocessor surface are the cause of this challenge. The proper approach is to cool these hotspots separately while maintaining the entire microprocessor surface at acceptable temperatures. A thermoelectric cooler module is suggested to be used to cool the hotspot. Thermoelectric generator modules are used to generate/harvest electrical power from the wasted heat of the microprocessor background, and then it is used to run the thermoelectric cooler. In this research, four parameters were used to develop a design tool to achieve the cooling system goals. These parameters are the height of the thermoelectric modules' legs, the spaces between the thermoelectric legs, the generated heat by the hotspot, and the generated heat by the microprocessor background. Simulated data were generated using a 3-D validated model. A neural network was then used to build the basis of a design tool, which can be improved to cover a wider range of parameters and their values. The results showed that the developed design tool in this study can be used to determine the proper parameters values for a given microprocessor temperature target.

Keywords: Microprocessor; hotspots; thermoelectric generator; thermoelectric cooler; neural network.

1. Introduction

The advances in microprocessor performance are based on increasing the chip packaging density. This began in the 1970s with a few transistors. The increase in the number of transistors that can be integrated in an Integrated Circuit (IC) has enormous value. For example, Figure 1 shows the trend of this advancement. In 2017, the number of packaged transistors surpassed 10 Giga.

The increase in chip components leads to a rapid increase in electrical power consumption and thus a dissipation of this power in the form of thermal heat. Thus, power consumption and dissipation are essential in the microprocessor design industry, which produces a real challenge. Microprocessors' cooling strategy is essential to the microprocessors manufacturing industry. It

is preferable to reduce power consumption. This is not only due to power cost but also because the power consumed must be dissipated. If access power is not dissipated, overheating would occur. The Complementary Metal–Oxide Semiconductor (CMOS) is the dominant technology in IC design due to its low static power consumption. Generated power in CMOS integrated circuits is due to three main sources: dynamic power, short circuit power, and leakage power. Eq (1) shows this relation.

$$P_{total} = P_{dynamic} + P_{short} + P_{leake} \quad (1)$$

Eq (2) shows the total power based on the dynamic and static power. Short circuits and leakage constitute static power, which makes Eq (1):

$$P_{total} = P_{dynamic} + P_{static} \quad (2)$$

The dynamic power is mainly generated during the charging and discharging of the capacitor connected to the output of the CMOS transistor.

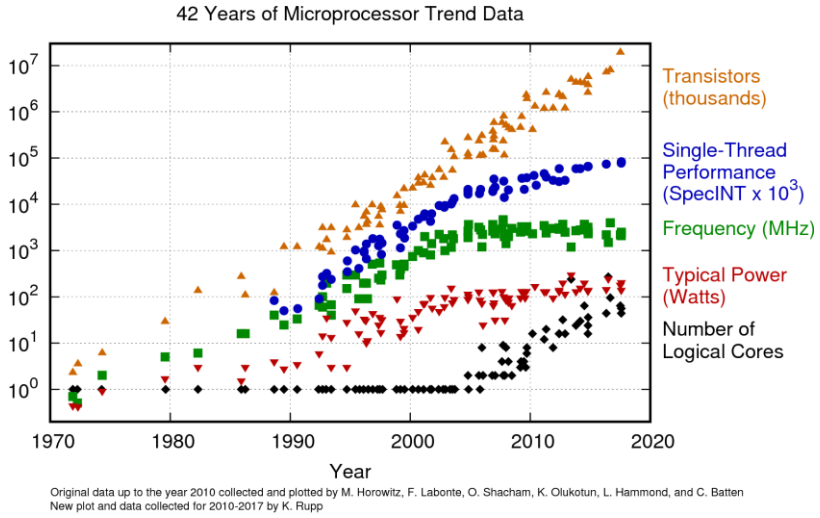


Fig. 1. 42 Years of Microprocessor Trend Data [1].

Advancements in the Very Large-Scale Integration (VLSI) design is mainly characterized by a large reduction in the transistor size. Downscaling is mainly in the form of transistor channel size reduction. About 30% of the IC reduction is obtained in each chip generation [2]. This results in a reduction of the supply voltage (V_{dd}), which in turn necessitates threshold voltage (V_{th}) reduction. The resulting effect is the significant increase in the leakage current, which leads to a considerable increase in static power; however, for each IC generation, the leakage current is increased five times [3]. Thus, although the dynamic power used is the dominant factor in power dissipation in processor design, the static power increases when the transistor size is reduced during fabrication. This is because the reduction in the transistor fabrication allows for supply power to be reduced, which in turn reduces dynamic power, but the leakage current increases, leading to a higher static power dissipation [4].

The microprocessor power generation depends on workload, technology, processor architecture, and operating systems. Power generation reduction can be obtained by varying methods starting from the circuit level to the architecture level, including the software management approach [4]. The static power is almost uniform in all the chip components, where its value depends mainly on the chip manufacturer. This is also the case for memory units, such as cache memory, various buffers, and low and high activity components. Because the dynamic power occurs during switching activity, its value varies from one chip component to another. Components with a high switching rate generate more dynamic power. For example, Results Broadcasting Bus (RBB) in Alpha 21364 core is one of the main components of high power dissipation [5]. The reorder buffer is also one of the main components in modern microprocessors that plays an important role in achieving a high performance. The reorder buffer consumes the highest power among all dynamically schedule processors [6]. Other components vary in power consumption [7]. In addition, the instructions to be executed have an influence on the switching activity. Thus, the values of the power consumption and the corresponding generated heat are application-dependent.

Memory-bound applications consume less power compared to compute-bound applications [8]. The instruction set of any microprocessor architecture can generally be divided into three main instructions groups: Arithmetic and Logic Unit (ALU), Load, and Store. Some instructions require more processor cycles, which in turn switch between ON and OFF states more often [6,7,9]. For example, instructions ADD, MUL, and NOP use different data path units and

consequently consume different amount of power [10]. The computation speed is affected by the Instruction Per Cycle (IPC). If a certain workload (program) encompasses a large amount of instructions with high processor cycles, the workload becomes a high power consumption program. This phenomenon generates heat that is highly non-uniform both temporally and spatially, which creates what is called hotpots [11,12]. These hotspots constitute a temperature gradient, which induces thermal stress, resulting in performance and reliability degradation. There are many proposed external cooling systems, such as cooling fans, water cooling, liquid nitrogen cooling, and microchannel cooling [13,14,15]; however, these cooling systems do not solve the problem of the temperature gradient on the microprocessor surface.

To prevent the microprocessor temperature from exceeding a threshold value, Dynamic Thermal Management (DTM) techniques have been developed. The main objective of DTM is to minimize the power dissipation while maximizing the microprocessor performance. There are three main DTM techniques: hardware, software, and architecture [9,16]. There are few hardware-based techniques used for thermal management control. Examples include Dynamic Voltage Scaling (DVS), Dynamic Voltage and Frequency Scaling (DVFS), power gating and clock gating, and these examples are among the most commonly used techniques. Reducing the supply voltage (V_{dd}) is achieved using the DVFS technique. There is a strong relation between the power supply (V_{dd}) and the microprocessor operating frequency, as shown in Figure 2. Supply voltage can be reduced up to a certain level, but beyond that, it will be not useful [14,18]. This is because the threshold voltage (V_{th}) should be reduced as well. On the other hand, the low V_{th} value generates more leakage currents and consequently increases the static power. Although reducing V_{dd} strongly reduces the power dissipation according to Eq (2), reducing V_{dd} reduces the frequency and vice versa [19]. As such, the execution performance of the microprocessor is greatly affected.

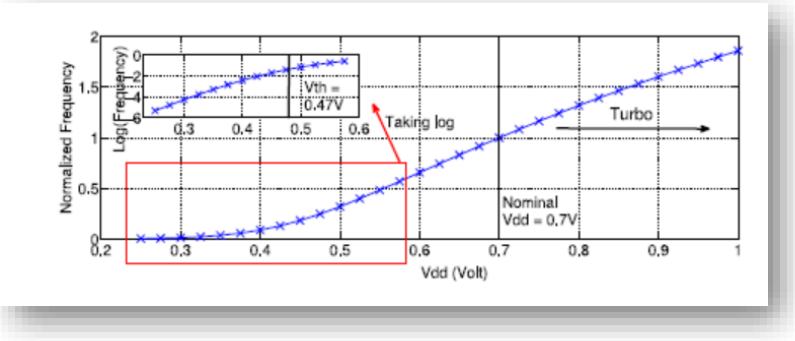


Fig. 2. Operating frequency under a wide range of V_{dd} [16 19].

It is important to point out that frequency downscaling is not preferable because it reduces the microprocessor performance. For the clock gating technique, the clock is stopped in certain components when they are not in use. This may not be a preferable solution as it requires extra control circuits and generates more heat to be dissipated. Also, the masked areas may not be returned to activity on time [20,21]. Similarly, for power gating, the power supply is shut-off on some chip components if they are not needed. Similar phenomena apply to clock gating [10,22]. The hardware solutions are effective in managing temperature, but they have a long execution time and a performance reduction as a result of frequency reduction, and they are global solutions that neglect the application-specific needs (e.g., see [9,23]).

As indicated, the generated microprocessor heat must be removed. Otherwise, the temperature of the microprocessor will exceed the acceptable threshold. Various manufacturers produce microprocessors with different threshold temperatures [2,24,25]. Another important phenomenon is that the temperature on the microprocessor surface is not uniform [26]. To the best of our knowledge, the best solution should be able to dissipate the generated heat from various microprocessor components and simultaneously ensure uniform temperature distribution on the surfaces of various microprocessor components, including the hotspot locations.

Using a validated 3-D model [27], a sustainable self-cooling technique using thermoelectric modules (TEMs) was suggested by Saber et al. [27] and Alshehri and Saber [28]. This technique is based on attaching a thermoelectric cooler (TEC) to the hotspot of the microprocessor. The rest of the cold microprocessor areas are attached to thermoelectric generator (TEG) modules.

These TEGs harvest electrical power from the microprocessor's wasted heat. This harvested electrical power is then used to run the TEC attached to the hotspot to cool it. It was found that in certain situations, the harvested electrical power generated by the TEGs was enough to run the TEC while reaching a hotspot temperature below the threshold value. Furthermore, with this technique, the temperature distribution of the entire microprocessor surface became approximately uniform. Because there is no need to external power requirements, this technique is referred to as a "sustainable self-cooling framework" for cooling microprocessor hotspots (see [26,28] for more details).

2. Microprocessor Cooling System

In this study, a design tool was developed for cooling microprocessor hotspots and was subjected to different operating conditions. This tool was developed based on the data obtained from a 3-D thermoelectric model that was previously developed by Saber et al. [27]. Briefly, the model solves the 3-D thermoelectric equations at both steady-state and transient conditions. This model can also be used for assessing and optimizing the thermal performance and electrical performance of cascaded and non-cascaded thermoelectric modules (TEMs) in both the thermoelectric cooler mode (TEC) and thermoelectric generator mode (TEG). Additionally, this model accounts for the thermal contact resistances and electrical contact resistances at all interfaces between materials layers of the TEM in both TEC and TEG modes. Lastly, the model handles the thermal properties and electrical properties of the TEM materials as temperature-dependent. To gain confidence in this model, it was extensively validated by comparing its predictions with experimental data of TEG and the experimental data of TEC. The model's predictions were in good agreement with the experimental data of the TEG of different operating conditions to within ± 3% and the experimental data of the TEC of different operating conditions to within ± 4%. The full details of the 3-D model and its capabilities are available from Saber et al. [27]. In several studies [28-31], the model was used to demonstrate the potential use of thermoelectric technology for cooling chip hotspots while maintaining its temperature at acceptable values.

2.1 System Simulation

To design a proper microprocessor cooling system, there are two main objectives. First, the hotspot temperature should not exceed the threshold temperature. Second, the temperature

distribution on the microprocessor surface should be kept as uniform as possible. To achieve these two goals, there are several parameters that can be manipulated to produce the cooling capability. In this research, four parameters were chosen to be manipulated. They are the P-/N-leg height of the TEM (h_{TEM}), the spacing between the P-/N-legs, which is called pitch (p_{TEM}), generated heat by the microprocessor background (Q_{TEG}), and generated heat by the hotspot (Q_{TEC}). The developed and validated 3-D model by Saber et al. [27] was extensively used in this study to generate simulated data with various values for the parameters shown in Table 1.

Table 1. Design parameters values used to conduct the simulations

h_{TEM} (µm)	**p_{TEM} (µm)**	Q_{TEG} (W)	Q_{TEC} (W)
24, 48	15, 30, 45	5, 10	20 to 40

Figure 3 shows a schematic of the simulated microprocessor and TEG and TEC placements. The simulated microprocessor was 15 mm x 15 mm. One thermoelectric cooler (TEC) was placed on the top of the middle part of the microprocessor where the hotspot was created. The rest of the microprocessor areas (24 in total) were covered by 24 TEGs, each of which had a size of 3 mm x 3 mm and generated heat at a heat rate called Q_{TEG}. The generated heat from the hotspot location is called Q_{TEC}. With all 24 TEGs of Q_{TEG} of 5 W, the dependence of the average hotspot temperature (T_{HS}) on the hotspot heat rate are provided in Figure 4. The corresponding results for the case of Q_{TEG}. of 10 W are provided in Figure 5.

TEG	TEG	TEC (hotspot)	TEG	TEG
TEG	TEG	TEG	TEG	TEG
TEG	TEG	TEG	TEG	TEG
TEG	TEG	TEG	TEG	TEG
TEG	TEG	TEG	TEG	TEG

Fig. 3. A schematic of 15 mm x 15 mm simulated microprocessor with TECs placed on the hotspot and TEGs placed on the background.

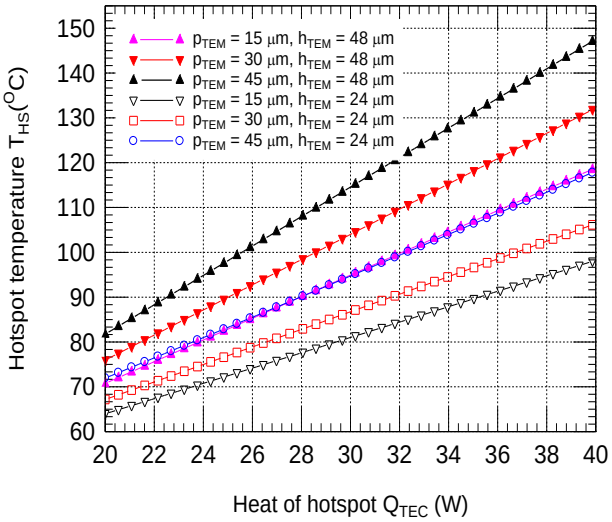


Fig. 4. Dependence of hotspot temperature on its heat rate (Q_{TEC}) at a background heat rate of Q_{TEG} of 5 W.

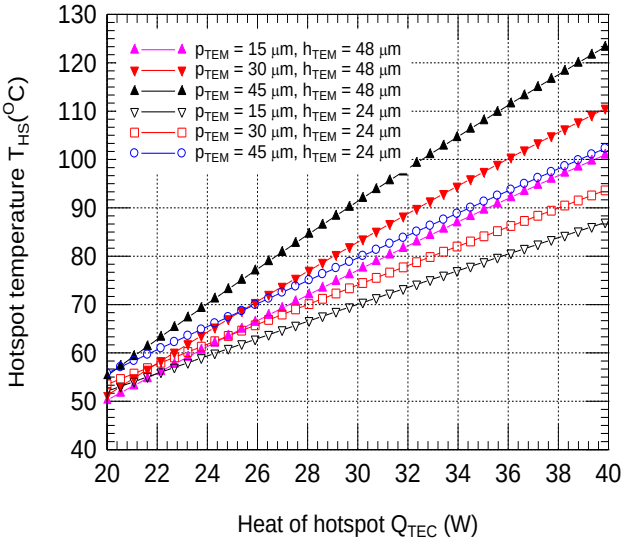


Fig. 5. Dependence of hotspot temperature on its heat rate (Q_{TEC}) at a background heat rate of Q_{TEG} of 10 W.

The threshold temperature varies for different microprocessor models and manufacturers [2,24,25]. The most common range is between 85 and 105°C. As shown in Figure 4, with p_{TEM} = 45 µm, h_{TEM} = 48 µm and Q_{TEG} = 5 W, the maximum Q_{TEC} that can be removed while keeping T_{HS} below a threshold temperature of 105°C is 27 W; however, with the same values of these parameters except for Q_{TEG} = 10 W, the hotspot temperature will not exceed the threshold temperature of 105°C until Q_{TEC} exceeds 34 W. This is because the harvested electrical power for the case of Q_{TEG} = 5 W is smaller than that for the case of Q_{TEG} = 10 W. As such, the TEC uses less electrical power for the case of Q_{TEG} = 5 W, resulting in removing less hotspot heat in relation to that for the case of Q_{TEG} = 10 W to reach the same hotspot temperature (i.e., 105°C).

2.2 Building the Tool Using a Neural Network

Using these data and the discussed scenario, the design tool for a microprocessor cooling system was developed using a neural network (NN). A feed-forward backpropagation neural network was trained, validated, and tested. In this NN, one hidden layer with three nodes was adequate to achieve a performance accuracy of 98.4 %. Figure 6 shows the main NN model and the 45-regression line with the correlation coefficient (R= 0.999).

The neural network principle is based on the following algorithm. Referring to Fig 6-a, the NN node activation function is:

$$net_j = \sum_i y_i * w_{ij}, \text{ where } y_i = f(net_j) \qquad (3)$$

where net_j is a neural network node. In Eq. (3), the transfer function $f(net_j)$ can be any nonlinear differentiable function. The logistic function ($(1 + e^{-x})^{-1}$) can be used. The errors are calculated as:

$$E = \frac{1}{2}\sum_j (t_j - y_j)^2, \qquad (4)$$

where t_j is the targeted output, and y_j is the predicted output. The errors are the output layer calculated as:

$$\frac{\partial E}{\partial y_j} = (y_j - t_j), \delta_j = \frac{\partial E}{\partial net_j}$$

$$= \frac{\partial E}{\partial y_j}.\frac{\partial y_j}{\partial net_j} = (y_j - t_j).f'(net_j) \qquad (5)$$

For node *i* in Eq. (5), the backpropagation error is calculated as:

$$\frac{\partial E}{\partial y_i} = \sum_j (\frac{\partial E}{\partial net_j}.\frac{\partial net_j}{\partial y_i}) = \sum_j (\delta_j . w_{ij}),\ \delta_i = \frac{\partial E}{\partial net_i} = \frac{\partial E}{\partial y_i}.\frac{\partial y_i}{\partial net_i} = \frac{\partial E}{\partial y_i}.f'(net_i)$$

(6)

Finally, the weights are updated as follows:

$$\frac{\partial E}{\partial w_{ij}} = \frac{\partial E}{\partial net_j}.\frac{\partial net_j}{\partial w_{ij}} = \delta_j.y_i,\ \Delta w_{ij} = -\mu.\frac{\partial E}{\partial w_{ij}} (7)$$

where μ in is the learning rate, which is between 0 and 1.0.

2.3 Tool Functionalities

The developed design tool in this study can be used to obtain four main tasks. This tool can be used as a calculator for determining T_{HS} as well as for identifying the values of the input parameters of h_{TEM}, p, Q_{TEG}, and Q_{TEC} to reach a target T_{HS}.

2.3.1 Calculating T_{HS}

The developed tool is used to calculate T_{HS} at each set of parameters values. In this case, when the values of all four input parameters are known in advance and only T_{HS} is needed, the values of these parameters are entered in a GUI in which the T_{HS} value is displayed accordingly. For demonstration purposes, Figure 7 shows three different examples with different sets on input parameters. T_{HS} can be obtained by specifying the four parameters, h_{TEM}, p_{TEM}, Q_{TEG}, and Q_{TEC}. These four parameters are the thermoelectric module design parameters. The designer can choose the proper design parameters to meet the T_{HS} maximum value. For example, h_{TEM} and p_{TEM} can be increased to ease the design without exceeding the THS maximum value.

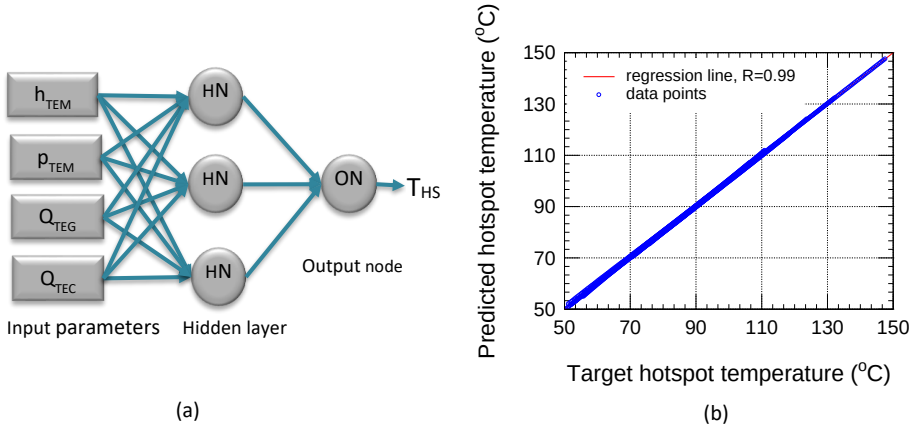
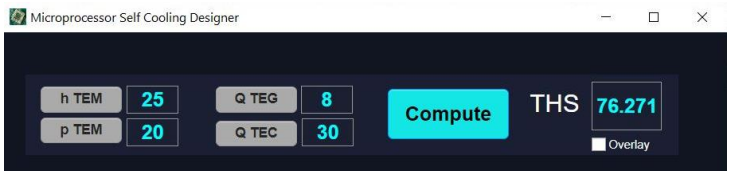


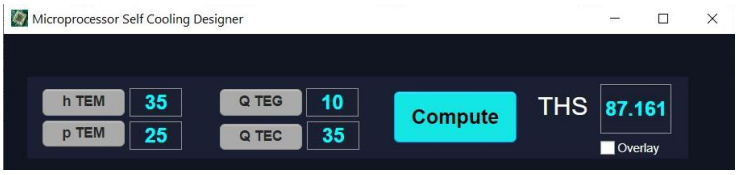
Fig. 6. Basic architecture of the designed NN: (a) the NN model with three hidden nodes (HN) and one output node (ON) for T_{HS} and (b) Predicted vs target T_{HS} produced by the trained NN.

2.3.2 T_{HS} Versus One Input Parameter

The developed design tool is also used to investigate the dependencies of the hotspot temperature, T_{HS}, on each input parameter when all other input parameters are set to specific values. This is important for identifying the TEMs that can be installed on the microprocessor surface (see Figure 3) to achieve a specified/target temperature at various operating conditions. For example, when it is necessary to investigate the effect of the h_{TEM} input parameter on T_{HS} while other input parameters are set to some fixed value, T_{HS} will be plotted versus h_{TEM} accordingly. Additionally, when one of the input parameters is changed and its effect needs to be observed, the tool will display the new curve as an overlay plot on the previous curves. For demonstration purposes for this feature, Figure 8 shows the relation between h_{TEM} and T_{HS} for two sets of fixed values of the other input parameters.



(a)



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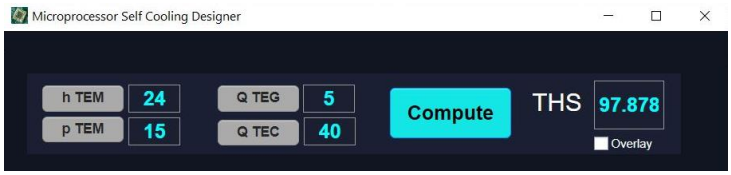

(c)

Fig. 7. Predicting the T_{HS} value from the rest of the parameter values.

2.3.3 Calculating Input Parameters – Design Mode

The tool can be effectively used to determine the values of the input parameters. In this case, it determines the optimum value of any of the four parameters in achieving the desired T_{HS} value. For example, when Q_{TEC} = 25 W, Q_{TEG} = 5 W and p_{TEM} = 30 µm, and the target T_{HS} is 75ºC, then the tool determines the h_{TEM} to be 32 µm. This basically means that the TEM height should be 32 µm to harvest the electrical power from the TEGs that is needed to run the TEC attached to the hotspot and to maintain its temperature at 75ºC. Other constraints on input parameter values can be used, and the tool will determine the left parameters to meet these constraints even when the number of the design parameters is two or three. Figure 9 shows how to determine each of

the four parameters. The red-colored background in the parameter area indicates the determined input parameter.

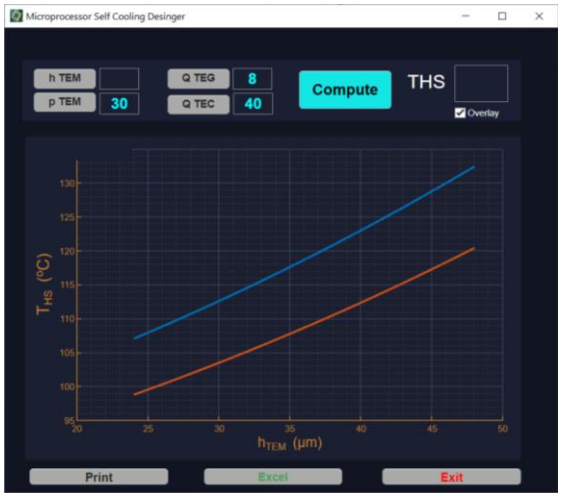

Fig. 8. T_{HS} vs h_{TEM} for p_{TEM} =30 µm, Q_{TEC}= 40 W, Q_{TEG} 5 W (blue curve), and 10 W (red curve).

2.3.4 T_{HS} Versus Two Input Parameters

The developed tool can be used to visualize the effect of two parameters on T_{HS} while fixing the other two parameters. As examples, Figures 10 and 11 show this effect in 3-D surface plots. Figure 10 shows T_{HS} versus both h_{TEM} and p_{TEM} at Q_{TEG} = 8 W. In the upper contour surface, Q_{TEC} is 35 W, while in the lower contour surface, Q_{TEC} is 40 W. The three parameters (h_{TEM}, p_{TEM}, and Q_{TEC}) can be easily determined from this figure to obtain a specified value for T_{HS}. Figure 11 shows a similar feature but when the values of h_{TEM} and p_{TEM} are fixed.

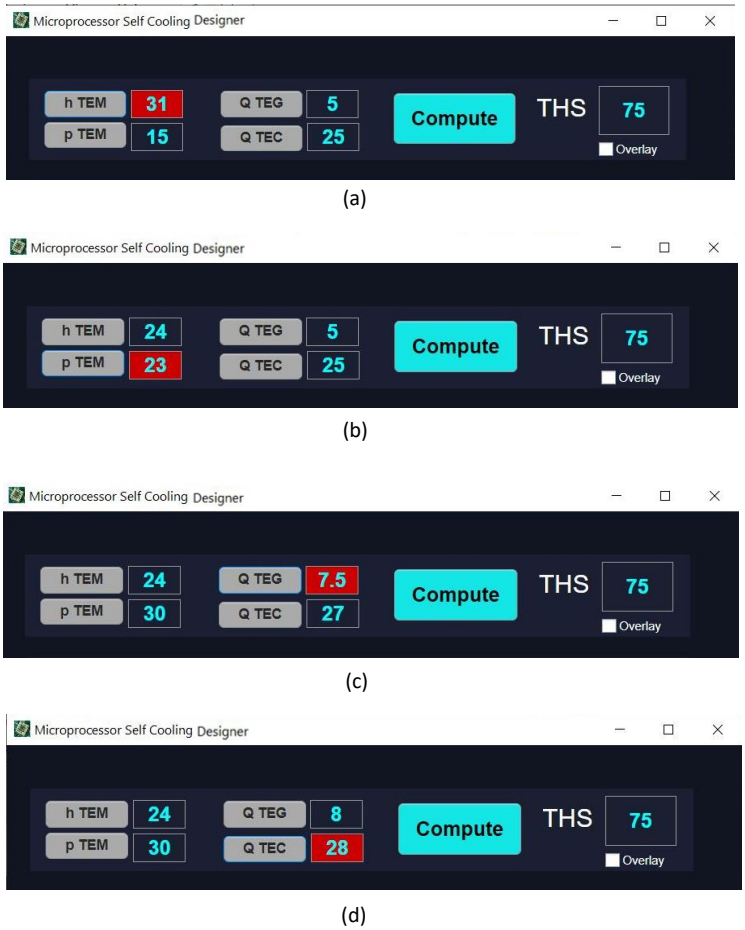

Fig. 9. Using the developed tool in the design mode to identify the values of the input parameters to achieve a target T_{HS}=75°C: (a) identifying h_{TEM}, (b) identifying p_{TEM}, (c) identifying Q_{TEG}, and (d) identifying Q_{TEC}.

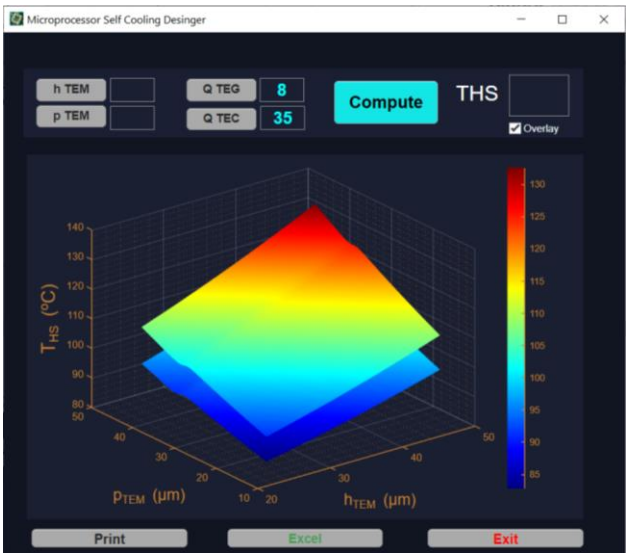

Fig. 10. T_{HS} vs both h_{TEM} and p_{TEM} at a fixed value of Q_{TEG} and (upper surface for Q_{TEC}=35 W while lower surface for Q_{TEC}=40 W).

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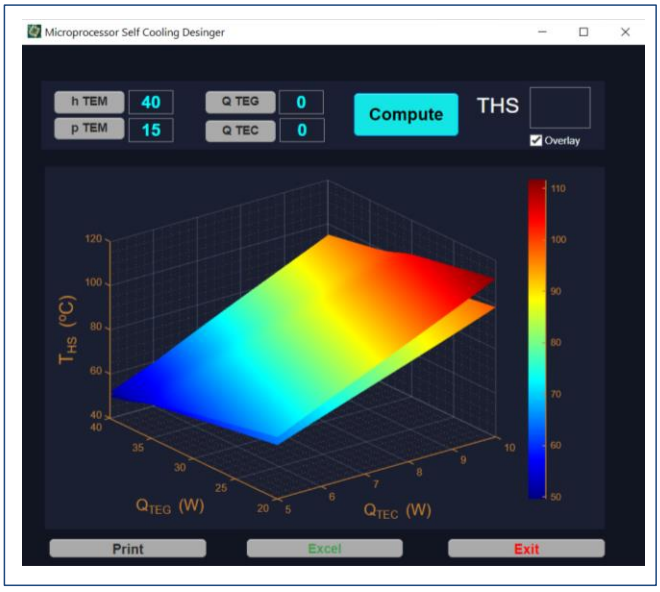

Fig. 11. T_{HS} vs both Q_{TEG} and Q_{TEC} at a fixed value of p_{TEM} and (upper surface for h_{TEM}=40 µm, while lower surface for h_{TEM}=25 µm).

3. Conclusion

Maintaining microprocessor temperatures under certain threshold values is an essential part of designing cooling systems. This involves removing the generated heat from primary hotspots and the background surface of the microprocessor. In this cooling system, a thermoelectric cooler (TEC) is used to cool the hotspot, and its electrical power is obtained from thermoelectric generators (TEGs). The TEGs harvest electrical power from the wasted heat on the cold surface of the microprocessor. Four main parameters allow the cooling system to reach the target microprocessor temperature. These parameters are the P-/N-leg height of the thermoelectric module, the spacing between thermoelectric module legs, the generated heat by hotspots, and the generated heat from the microprocessor background. A set of simulations of the cooling system was generated using a 3-D thermoelectric model that was previously developed and validated against experimental data from both TEC and TEG. The obtained results were used to create a neural network predictor. A user-friendly GUI was developed to integrate all the system design input and output parameters. The developed tool can be used in two modes: (a) determining the hotspot temperature for the given values of the four parameters and (b) identifying the values of the input parameters to reach a specified temperature for the hotspot. The use of the developed design tool can be easily extended to different types of microprocessors and subjected to various operating conditions.

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تطوير أداة تصميم لتبريد النقاط الساخنة للمعالج الدقيق باستخدام وحدات الكهروحراريات

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ملخص البحث. من الصعب الحفاظ على درجة حرارة سطح المعالج الدقيق موزعة بالتساوي وأقل من قيمة العتبة باستخدام أساليب التبريد الإلكترونية التقليدية. النقاط الساخنة على سطح المعالج الدقيق هي سبب هذا التحدي. الطريقة الصحيحة هي تبريد هذه النقاط الساخنة بشكل منفصل مع الحفاظ على سطح المعالج الدقيق بأكمله عند درجات حرارة مقبولة. يُقترح استخدام وحدة تبريد حرارية لتبريد النقطة الساخنة. تُستخدم وحدات المولدات الكهروحرارية لتوليد وحصاد الطاقة الكهربائية من الحرارة الضائعة لسطح المعالجات الدقيقة ، ثم يتم استخدامها لتشغيل المبرد الكهروحراري. في هذا البحث ، تم استخدام أربعة متغيرات لتطوير وتصميم أداة لتحقيق أهداف نظام التبريد. هذه المتغيرات هي ارتفاع أرجل الوحدات الحرارية ، والمسافات بين الأرجل الكهروحرارية ، والحرارة المتولدة من النقطة الساخنة ، والحرارة الناتجة من سطح المعالج الدقيق. تم إنشاء البيانات المحاكاة باستخدام نموذج ثلاثي الأبعاد تم التحقق منه. ثم تم استخدام الشبكة العصبية الصناعية لبناء أساس أداة التصميم ، والتي يمكن تحسينها لتغطية نطاق أوسع من المتغيرات وقيمها. أظهرت النتائج أنه يمكن استخدام أداة التصميم المطورة في هذه الدراسة لتحديد قيم المتغيرات المناسبة للوصول الى درجة حرارة معالج دقيق معينة.